Claims

[c1] 1.A method of displaying a guard ring within an integrated circuit design having logic devices, said method comprising:
determining positions of said logic devices within said integrated circuit design;
incorporating said guard ring into said integrated circuit design; and
displaying said logic devices and said guard ring one of graphically, semantically, and symbolically in a single display.

[c2] 2.The method in claim 1, wherein said displaying of said logic devices and said guard ring symbolically comprises displaying a parameterized symbol.

[c3] 3.The method in claim 2, wherein said displaying of said parameterized symbol displays parameters including the type of circuit and the type of guard ring.

[c4] 4.The method in claim 2, wherein said displaying of said parameterized symbol displays parameters including the efficiency of said guard ring.

[c5] 5.The method in claim 1, wherein said displaying of said logic devices and said guard ring graphically comprises illustrating relative positions of said logic devices and said guard ring.

[c6] 6. A method of incorporating a guard ring into an integrated

circuit design having logic devices, said method comprising:
identifying the type of circuit created by said logic devices;
selecting a type of guard ring based on said type of circuit;
incorporating said type of guard ring into said integrated circuit design; and
verifying the operation of said guard ring within said integrated circuit design.

[c7] 7.The method in claim 6, further comprising adding an electrostatic discharge (ESD) protection circuit to said integrated circuit design to protect said logic devices and identifying the type of ESD protection circuit added, wherein said process of selecting said type of guard ring is further based on said type of ESD protection circuit identified.

[c8] 8.The method in claim 7, wherein said type of ESD protection circuit comprises one of an input type, a power clamp type, and a type.

[c9] 9.The method in claim 6, wherein said type of circuit comprises one of a radio frequency (RF) circuit, a digital circuit, and an analog circuit.

[c10] 10.The method in claim 6, further comprising automatically adjusting the size and position of said guard ring as the size of said integrated circuit design is changed.

[c11] 11 The method in claim 6, further comprising adjusting said

guard ring based on guard ring efficiency requirements.

[c12] 12The method in claim 6, wherein said type of guard ring includes an enclosed guard ring with n-well rings, deep trench (DT), trench isolation (TI), p+ diffusion rings, and n+ diffusion rings.

[c13] 13. A method of displaying at least one guard ring within a hierarchical integrated circuit design having logic devices, said method comprising:
establishing positions of said logic devices within a portion of said hierarchical integrated circuit design;
incorporating said guard ring into said portion of said hierarchical integrated circuit design; and
displaying said portion of said integrated circuit design as a cell having a guard ring within said hierarchical integrated circuit design.

[c14] 14. The method in claim 13, wherein said displaying of said portion of said integrated circuit design comprises symbolically displaying a parameterized symbol.

[c15] 15.The method in claim 14, wherein said displaying of said parameterized symbol displays parameters including the type of circuit and the type of guard ring.

[c16] 16.The method in claim 14, wherein said displaying of said parameterized symbol displays parameters including the

efficiency of said guard ring.

[c17] 17.The method in claim 13, wherein said displaying of said portion of said integrated circuit design comprises graphically illustrating relative positions of said logic devices and said guard ring.

[c18] 18.A method of incorporating at least one guard ring into a hierarchical integrated circuit design, said method comprising:
identifying the type of circuit located within a portion of said hierarchical integrated circuit design;
selecting a type of guard ring based on said type of circuit;
incorporating said type of guard ring into said portion of said hierarchical integrated circuit design;
verifying the operation of said guard ring within said portion of said hierarchical integrated circuit design; and
replacing said portion of said integrated circuit design with a cell having a guard ring within said hierarchical integrated circuit design.

[c19] 19.The method in claim 18, further comprising adding an electrostatic discharge (ESD) protection circuit to said integrated circuit design and identifying the type of ESD protection circuit added, wherein said process of selecting said type of guard ring is further based on said type of ESD protection circuit identified.

[c20] 20.The method in claim 19, wherein said type of ESD protection circuit comprises one of an input type, a power clamp type, and a rail to rail type.

[c21] 21.The method in claim 18, wherein said type of circuit comprises one of a radio frequency (RF) circuit, a digital circuit, and an analog circuit.

[c22] 22.The method in claim 18, further comprising automatically adjusting the size and position of said guard ring as the size of said integrated circuit design is changed.

[c23] 23. The method in claim 18, further comprising adjusting said guard ring based on guard ring efficiency requirements.

[c24] 24.The method in claim 18, wherein said type of guard ring includes an enclosed guard ring with n-well rings, deep trench (DT), trench isolation (TI), p+ diffusion rings, and n+ diffusion rings.

[c25] 25.A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of displaying a guard ring within an integrated circuit design having logic devices, said method comprising:

determining positions of said logic devices within said integrated circuit design;

incorporating said guard ring into said integrated circuit

design; and

displaying said logic devices and said guard ring one of graphically, semantically, and symbolically in a single display.

[c26] 26.The method in claim 25, wherein said displaying of said logic devices and said guard ring symbolically comprises displaying a parameterized symbol.

[c27] 27.The program storage device in claim 26, wherein said displaying of said parameterized symbol displays parameters including the type of circuit and the type of guard ring.

[c28] 28.The program storage device in claim 26, wherein said displaying of said parameterized symbol displays parameters including the efficiency of said guard ring.

[c29] 29.The program storage device in claim 25, wherein said displaying of said logic devices and said guard ring graphically comprises illustrating relative positions of said logic devices and said guard ring.